IN THE SPECIFICATION

Please replace the paragraph on page 1, lines 14-20, with the following amended paragraph:

The present patent application is related to co-pending and commonly owned U.S. Patent Application No. 10/038,209 ~~XX/XXX,XXX~~, Attorney Docket No. POU920010165US1, entitled "Delay Correlation Analysis and Representation for VITAL Compliant VHDL Models", and U.S. Patent Application No. 10/038,311 ~~XX/XXX,XXX~~, Attorney Docket No. POU920010005US1, entitled "Size Reduction Techniques for VITAL Compliant VHDL Simulation Models", filed on even date with the present patent application, the entire teachings of which being hereby incorporated by reference.

PAGE 2/20 * RCVD AT 10/14/2005 10:30:29 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/25 * DNIS:2738300 * CSID: * DURATION (mm-ss):06-56

Please replace the paragraph on page 22, lines 1-10, with the following amended paragraph:

A [[a]] typical tuple ~~$X_1Y_1Z_1$~~ $Z_1X_1Y_1$ for a two input AND gate would be {5,6,40}, where 5 is the entry for a two input AND gate topology, and 6 is the number of generics, and 40 would indicate a maximum of 40 unique delay values in the correlation set. The X_1 value of 6 is defined by the gate topology, the Z_1 and Y_1 values would vary, based on the processing order (Z_1) and delay correlation (Y_1). A larger gate (e.g. Latch) topology would have a different delay correlation capacity identified by $Z_2X_2Y_2$ tuple {2,20,60} (Logic gate topology 2, Total of 20 generics defined, Total of 60 unique delay values utilized in this correlation set). The following calculations demonstrate the efficiencies of using this variable structure approach versus a uniform dimension array *for just two entries*:

Please replace the paragraph on page 22, line 24, with the following:

(X_1 * Y_1) slots * 4 bytes/slot ~~4/bytes/slot~~ = (6) * (40) * 4 = 960 bytes

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